REMARKS

In response to the Office Action mailed on June 2, 2006, Applicants respectfully request reconsideration. Claims 1-6 and 24-31 are now pending in this Application. Claims 1 and 24 are independent claims and the remaining claims are dependent claims. Claims 30 and 31 have been added. A version of the claims are attached hereinabove. Applicants believe that the claims as presented are in condition for allowance. A notice to this affect is respectfully requested.

Claims 1 and 24 were rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6523135 to Nakamura (hereinafter Nakamura. Applicants respectfully disagree with these contentions and assert that the present claimed invention is not anticipated by any disclosure in the Nakamura reference.

Claim 1 recites in part "...a conversion circuit to convert the physical address in the memory array to a logical address in the memory array to allow said test vector to be written to said logical address of the memory array."

The Examiner stated that Nokamura teaches the same by way of a bitmap converter 16. Applicants respectfully disagree with the Examiner's statement. Nokamura states at column 4, lines 53-55 that the bitmap converter 16 is used to provide write data "din" and output data "dout" from the Ram interface 13 to the DRAM 127. Further, at column 5, lines 8-14, Nokamura describes the bitmap converter functions to invert the logical value based on the physical condition of the DRAM and for delivering the data "Dout" as it is or after converting the data into bit mapped data out. Further still at column 8, lines 53-60, the bitmap converter reverses the read data "dout" from a "0" to a "1" or from a "1" to a "0". The bitmap converter also reverses the write data if it is instructed to do so. Thus, the bitmap converter of Nokamura converts the data, not the address therefore Nokamura fails to disclose or suggest a conversion circuit to convert the physical address in the memory array to a logical address in the memory array to allow said test vector to be written to said logical address of the

memory array. Therefore, claim 1 is believed allowable over Nokamura. Claim 24 contains similar language as claim 1 and is believed allowable for the same reasons as claim 1. Accordingly, the rejection of claims 1 and 24 under 35 U.S.C. § 102(e) is believed to have been overcome.

Claims 2-6 and 25-29 were rejected under 35 U.S.C. §103 as being obvious over Nakamura. Claims 2-6 and 25-29 depend from claims 1 or 24 and are believed allowable as they depend from a base claim which is believed allowable. Accordingly, the rejection of claims 2-6 and 25-29 under §103 is believed to have been overcome.

Claims 30 and 31 have been added. Support for claims 30 and 31 can be found throughout the specification, for example at page 8, lines 10-21. Applicants submit that no new matter has been added by the addition of claims 30-31 and the prior art of record fails to disclose or suggest the subject matter of claims 30-31.

In view of the above, the Examiners rejections are believed to have been overcome, placing claims 1-6 and 24-31 in condition for allowance and reconsideration and allowance thereof is respectfully requested.

Applicants hereby petition for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-3735.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 616-9660, in Westborough, Massachusetts.

Respectfully submitted,

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